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09/766,846	01/23/2001	Hiroki Shinkawata	50090-275	1557

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EXAMINER
VU, HUNG K

ART UNIT	PAPER NUMBER
2811	

DATE MAILED: 07/26/2002

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)
	09/766,846	SHINKAWATA, HIROKI
	Examiner	Art Unit
	Hung K. Vu	2811

-- The MAILING DATE of this communication appears on the cover sh t with th correspond nc address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *14 May 2002* .

2a)☒ This action is FINAL. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-20* is/are pending in the application.

4a) Of the above claim(s) *16-20* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-15* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

Claim Rejections - 35 USC § 102

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (a) the invention was known or used by others in this country, or patented or described in a printed publication in this or a foreign country, before the invention thereof by the applicant for a patent.

Claims 1-2 and 15-16 are rejected under 35 U.S.C. 102(a) as being anticipated by Sung (PN 6,137,130, of record).

Sung discloses, as shown in Figures 4A-4B and 6B, a semiconductor device comprising,

transfer gates (44);

contact plugs (50) adjacent to the transfer gates;

each transfer gate having a gate insulating film (3), a gate electrode (4), and sidewalls for covering sides of the gate insulating film and the gate electrode layer;

each contact plug having the same height as the transfer gate and adjacent to the transfer gate over the whole height;

first interlayer insulating film having a surface which defines the same surface as the surface of the transfer gate and the surface of the contact plug;

a second interlayer insulating film (12) formed on the first interlayer insulating film;

diameter-reduced contact plugs which are smaller than the contact plugs and extend through the second interlayer insulating film to conduct to the contact plugs, respectively.

With regard to claim 2, Sung discloses the device further including a memory cell section having a plurality of memory cells,

the memory cell section including, in addition to the transfer gates, the contact plugs, and the first and second interlayer insulating films,

a bit line (14) formed on the second interlayer insulating film;

a third interlayer insulating film (52) formed on the second interlayer insulating film so as to cover the bit line;

capacitors formed on the third interlayer insulating film;

the memory cell section further including, as the diameter-reduced contact plugs, which include

a bit line contact plug which extends through the second interlayer insulating film to bring the contact plugs and the bit line into conduction;

capacitor contact plugs which extend through the second and third interlayer insulating films to bring the contact plugs and the capacitor into conduction.

With regard to claims 15 and 16, Sung discloses the gate insulating film of the transfer gate is silicon oxide. Note that the terms "a CVD insulating film formed by a CVD method" and "a thermal oxide film formed by a thermal oxidation method or a thermally-oxidized nitride film formed by a thermal oxidation nitriding method" are method recitations in a device claimed, and they are non-limiting, because only the final product is relevant, not the method of making. A product by process claim is directed to the product per se, no matter how actually made. See also

MPEP 2113. Moreover, an old or obvious product produced by a new method is not a patentable product, whether claimed in "product by process" claims or not.

2. Claims 1-2 and 15-16 are rejected under 35 U.S.C. 102(a) as being anticipated by Hosotani et al. (PN 6,051,859, of record).

Hosotani et al. discloses, as shown in Figures 2B, 2J and 5-6, a semiconductor device comprising,

transfer gates;

contact plugs (10,11) adjacent to the transfer gates;

each transfer gate having a gate insulating film (not shown), a gate electrode (3), and sidewalls (7) for covering sides of the gate insulating film and the gate electrode layer;

each contact plug having the same height as the transfer gate and adjacent to the transfer gate over the whole height;

first interlayer insulating film (8) having a surface which defines the same surface as the surface of the transfer gate and the surface of the contact plug;

a second interlayer insulating film (12) formed on the first interlayer insulating film;

diameter-reduced contact plugs which are smaller than the contact plugs and extend through the second interlayer insulating film to conduct to the contact plugs, respectively.

With regard to claim 2, Hosotani et al. discloses the device further including a memory cell section having a plurality of memory cells,

the memory cell section including, in addition to the transfer gates, the contact plugs, and the first and second interlayer insulating films,

a bit line (14) formed on the second interlayer insulating film;

a third interlayer insulating film (15) formed on the second interlayer insulating film so as to cover the bit line;

capacitors formed on the third interlayer insulating film;

the memory cell section further including, as the diameter-reduced contact plugs, which include

a bit line contact plug (13) which extends through the second interlayer insulating film to bring the contact plugs and the bit line into conduction;

capacitor contact plugs which extend through the second and third interlayer insulating films to bring the contact plugs and the capacitor into conduction.

With regard to claims 15 and 16, Hosotani et al. discloses the gate insulating film of the transfer gate is silicon oxide. Note that the terms "a CVD insulating film formed by a CVD method" and "a thermal oxide film formed by a thermal oxidation method or a thermally-oxidized nitride film formed by a thermal oxidation nitriding method" are method recitations in a device claimed, and they are non-limiting, because only the final product is relevant, not the method of making. A product by process claim is directed to the product per se, no matter how actually made. See also MPEP 2113. Moreover, an old or obvious product produced by a new method is not a patentable product, whether claimed in "product by process" claims or not.

Claim Rejections - 35 USC § 103

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 3-12 are rejected under 35 U.S.C. 103(a) as being unpatentable over Sung (PN 6,025,227, of record) in view of Ozaki et al. (PN 6,104,052, of record).

With regard to claims 3 and 12, Sung and Ozaki et al. discloses the gate electrode layer has a doped silicon layer containing an impurity and a silicide film for covering the surface of the doped silicon layer, any of the contact plugs corresponding to the capacitors, the capacitor contact plugs, and lower electrodes of the capacitors is formed of doped silicon containing an impurity, the contact plug corresponding to the bit line has a doped silicon layer containing an impurity, and bit line contact plug has a barrier metal brought into contact with the each contact plug and a metal layer formed on the barrier metal. Sung and Ozaki et al. do not disclose a silicide film formed only at a portion brought into contact with the bit line contact plug. However, it would have been obvious to one of ordinary skill in the art at the time the invention was made to form the device of Sung and Ozaki et al. having a silicide form between the bit line contact plug and the contact plug in order to reduce the contact resistance between the bit line contact plug and the contact plug.

With regard to claims 4, 7, 8, and 11, Sung and Ozaki et al. disclose all of the claimed limitations except material of a capacitor insulating film, an upper electrode, contact plugs and gate electrode layers of NMOS and PMOS transistors. However, it would have been obvious to one of ordinary skill in the art at the time the invention was made to form the device of Sung and Ozaki et al. having the materials as that claimed by Applicant, since it has been held to be within the general skill of a worker in the art to select a known material on the basis of its suitability for the intended use as a matter of obvious design choice. *In re Leshin*, 125 USPQ 416.

With regard to claims 5 and 9, Sung discloses a DRAM section having all of the claimed limitations. Sung does not disclose the device further including a logic circuit section, wherein the logic circuit section including a plurality of transistors, in addition to the transfer gates, the contact plugs, and the first and second interlayer insulating films, bit lines formed on the second interlayer insulating films, diameter-reduced contact plugs. However, Ozaki et al. discloses the device comprising a DRAM section and a logic circuit section, wherein the logic circuit section including a plurality of transistors, in addition to the transfer gates, the contact plugs, and the first and second interlayer insulating films, bit lines formed on the second interlayer insulating films, diameter-reduced contact plugs. Note Figures 3A – 15G (especially Figure 14G) of Ozaki et al.. Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to form the device of Sung having a logic circuit section, wherein the logic circuit section including a plurality of transistors, in addition to the transfer gates, the contact plugs, and the first and second interlayer insulating films, bit lines formed on the second

interlayer insulating films, diameter-reduced contact plugs, such as taught by Ozaki et al. in order to control the DRAM section to perform the desire function.

With regard to claims 6 and 10, Sung and Ozaki et al. disclose the logic circuit section has NMOS transistors and PMOS transistors both of which constitute CMOS transistors.

4. Claims 3-12 are rejected under 35 U.S.C. 103(a) as being unpatentable over Hosotani et al. (PN 6,051,859, of record) in view of Ozaki et al. (PN 6,104,052, of record).

With regard to claims 3 and 12, Hosotani et al. and Ozaki et al. disclose the gate electrode layer has a doped silicon layer containing an impurity and a silicide film for covering the surface of the doped silicon layer, any of the contact plugs corresponding to the capacitors, the capacitor contact plugs, and lower electrodes of the capacitors is formed of doped silicon containing an impurity, the contact plug corresponding to the bit line has a doped silicon layer containing an impurity, and bit line contact plug has a metal layer. Hosotani et al. and Ozaki et al. do not disclose a silicide film formed only at a portion brought into contact with the bit line contact plug. However, it would have been obvious to one of ordinary skill in the art at the time the invention was made to form the device of Hosotani et al. and Ozaki et al. having a silicide form between the bit line contact plug and the contact plug, the barrier surround the metal in order to reduce the contact resistance between the bit line contact plug and the contact plug, and to prevent the impurity from diffusing into the metal.

With regard to claims 4, 7, 8, and 11, Hosotani et al. and Ozaki et al. disclose all of the claimed limitations except material of a capacitor insulating film, an upper electrode, contact plugs and gate electrode layers of NMOS and PMOS transistors. However, it would have been obvious to one of ordinary skill in the art at the time the invention was made to form the device of Hosotani et al. and Ozaki et al. having the materials as that claimed by Applicant, since it has been held to be within the general skill of a worker in the art to select a known material on the basis of its suitability for the intended use as a matter of obvious design choice. *In re Leshin*, 125 USPQ 416.

With regard to claims 5 and 9, Hosotani et al. discloses a DRAM section having all of the claimed limitations. Hosotani et al. does not disclose the device further including a logic circuit section, wherein the logic circuit section including a plurality of transistors, in addition to the transfer gates, the contact plugs, and the first and second interlayer insulating films, bit lines formed on the second interlayer insulating films, diameter-reduced contact plugs. However, Ozaki et al. discloses the device comprising a DRAM section and a logic circuit section, wherein the logic circuit section including a plurality of transistors, in addition to the transfer gates, the contact plugs, and the first and second interlayer insulating films, bit lines formed on the second interlayer insulating films, diameter-reduced contact plugs. Note Figures 3A – 15G (especially Figure 14G) of Ozaki et al.. Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to form the device of Hosotani et al. having a logic circuit section, wherein the logic circuit section including a plurality of transistors, in addition to the transfer gates, the contact plugs, and the first and second interlayer insulating films, bit lines

formed on the second interlayer insulating films, diameter-reduced contact plugs, such as taught by Ozaki et al. in order to control the DRAM section to perform the desire function.

With regard to claims 6 and 10, Hosotani et al. and Ozaki et al. disclose the logic circuit section has NMOS transistors and PMOS transistors both of which constitute CMOS transistors.

5. Claim 13 is rejected under 35 U.S.C. 103(a) as being unpatentable over Sung (PN 6,025,227, of record) in view of Lou (PN 6,093,590, of record).

Sung discloses all of the claimed limitations except the gate electrode layer has a metal layer and a barrier metal which surrounds the metal layer. However, Lou discloses the gate electrode layer has a metal layer (118a) and a barrier metal (116a) which surrounds the metal layer. Therefore it would have been obvious to one of ordinary skill in the art at the time the invention was made to form the gate electrode layer of Sung having a metal layer and a barrier metal which surrounds the metal layer, such as taught by Lou because metal gate has a low sheet resistance so that the word line delay is effectively reduced.

6. Claim 13 is rejected under 35 U.S.C. 103(a) as being unpatentable over Hosotani et al. (PN 6,051,859, of record) in view of Lou (PN 6,093,590, of record).

Hosotani et al. discloses all of the claimed limitations except the gate electrode layer has a metal layer and a barrier metal which surrounds the metal layer. However, Lou discloses the gate electrode layer has a metal layer (118a) and a barrier metal (116a) which surrounds the metal layer. Therefore it would have been obvious to one of ordinary skill in the art at the time the

invention was made to form the gate electrode layer of Hosotani et al. having a metal layer and a barrier metal which surrounds the metal layer, such as taught by Lou because metal gate has a low sheet resistance so that the word line delay is effectively reduced.

Response to Arguments

7. Applicant's arguments filed 5/14/02 have been fully considered but they are not persuasive.

It is argued, at pages 4-6 of the Remarks, that Sung does not disclose a first insulating film has a surface which defines the same surface as the surface of a transfer gate and the surface of a contact plug, as recited in claim 1. This argument is not convincing because Sung teaches, as shown in Figures 4A-4B and 5A-5B, a first insulating film (2) has a surface which defines the same surface as the surface of a transfer gate (44) and the surface of a contact plug (50). Note that the gate electrode (4,5) and the cap (6) are parts of the transfer gate (44).

It is argued, at pages 6, 8 and 12 of the Remarks, that the Examiner is assuming that a CVD film or a thermal oxidation film are identical films regardless of the process used to form the film and this assumption is incorrect. This argument is not convincing because the Examiner does not state that these films are identical nor structurally indistinct, but state that the terms "a CVD insulating film formed by a CVD method" and "a thermal oxide film formed by a thermal oxidation method or a thermally-oxidized nitride film formed by a thermal oxidation nitriding method" are method recitations in a device claimed, and they are non-limiting, because only the final product is relevant, not the method of making. Therefore, a product by process claim is

directed to the product per se, no matter how actually made. See also MPEP 2113. Moreover, an old or obvious product produced by a new method is not a patentable product, whether claimed in "product by process" claims or not. Noted that in the specification, Applicant just discloses that the gate insulating film is formed by CVD or thermal oxidation. There is nothing in the specification mentions that CVD is more advantage than thermal oxidation, or vice versa. In this case, it is noted that Sung also discloses, at Col. 3, lines 5-7, a formation of gate insulating film (3) by a thermal oxidation method.

It is argued, at pages 7-8 of the Remarks, that Hosotani does not disclose a first insulating film has a surface which defines the same surface as the surface of a transfer gate and the surface of a contact plug, as recited in claim 1, because of a capping layer 7 over the gate electrode 3. This argument is not convincing because Hosotani teaches, as shown in Figures 3A-3D, a first insulating film (8) has a surface which defines the same surface as the surface of a transfer gate and the surface of a contact plug (10). Note that the gate electrode (3) and the cap (7) are parts of the transfer gate.

It is argued, at page 10 and 12 of the Remarks, that the Examiner does not provide any source to teach a silicide layer and a barrier layer, as recited in claims 3 and 12. Accordingly, Applicant's Admitted Prior Art Figure 27A and Tanaka (PN 6,369,446) are cited to support the well-known position.

It is argued, at pages 10 and 12 of the Remarks, that the Examiner does not provide any source to teach the known material. Accordingly, Hsu et al. (PN 5,693,974), Agnello et al. (PN 5,796,166), and Chen et al. (PN 6,100,137) are cited to support the well-known position.

It is argued, at pages 11-12 of the Remarks, that the motivation "to control the DRAM section to perform the desire function" is not sufficient to establish a prima facie case of obviousness. This argument is not convincing because it is well-known in the semiconductor art that DRAM includes a memory cell section and the logic section, and that the logic section is used to control the memory cell section to perform the desire function (providing power, filter, rectify, etc.).

It is argued, at page 13 of the Remarks, that Sung does not disclose the limitations of claim 1, therefore, Sung in view of Lou do not disclose the limitation of claim 13. This argument is not convincing for the reason as previously stated. Since Applicant's claim 1 does not distinguish over the Sung reference, therefore, Applicant's claim 13 does not distinguish over the Sung in view of Lou reference.

It is argued, at pages 13-14 of the Remarks, that Hosotani does not disclose the limitations of claim 1, therefore, Hosotani in view of Lou do not disclose the limitation of claim 13. This argument is not convincing for the reason as previously stated. Since Applicant's claim 1 does not distinguish over the Hosotani reference, therefore, Applicant's claim 13 does not distinguish over the Hosotani in view of Lou reference.

Conclusion

8. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Hung K. Vu whose telephone number is (703) 308-4079. The examiner can normally be reached on Mon-Thurs 7:00-5:30, Eastern Time.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Tom Thomas can be reached on (703) 308-2772. The fax phone numbers for the organization where this application or proceeding is assigned are (703) 308-7722 for regular communications and (703) 308-7722 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703) 308-0956.

Vu

July 22, 2002

Tom Thomas

TOM THOMAS
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